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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,877	12/23/1999	ADRIAN SFARTI	0100.9910145	8063
	7590 07/23/200 MICRO DEVICES, INC	EXAMINER		
C/O VEDDER PRICE P.C. 222 N.LASALLE STREET			FAHERTY, COREY S	
CHICAGO, IL			ART UNIT	PAPER NUMBER
			2183	
			MAIL DATE	DELIVERY MODE
			07/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)			
Office Action Occurrence		09/471,877	SFARTI ET AL.			
	Office Action Summary	Examiner	Art Unit			
		Corey S. Faherty	2183			
Period fo	The MAILING DATE of this communication app or Reply	pears on the cover sheet with the c	correspondence address			
WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLECHEVER IS LONGER, FROM THE MAILING DESIGNS of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. Properties of the period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION (36(a). In no event, however, may a reply be tirwill apply and will expire SIX (6) MONTHS from (6), cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).			
Status						
1) 又	Responsive to communication(s) filed on 30 Ju	une 2009				
-	This action is <b>FINAL</b> . 2b) ☐ This action is non-final.					
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
٥,١	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Dispositi	on of Claims					
4)⊠	☑ Claim(s) <u>7,10,11,14,17,20-27 and 34-38</u> is/are pending in the application.					
·—	4a) Of the above claim(s) is/are withdrawn from consideration.					
	☐ Claim(s) <u>20-27 and 34-38</u> is/are allowed.					
	∑ Claim(s) <u>7,10,11,14 and 17</u> is/are rejected.					
· ·	Claim(s) is/are objected to.					
•	Claim(s) are subject to restriction and/o	or election requirement.				
Applicati	on Papers					
9)☐ The specification is objected to by the Examiner.						
•	The drawing(s) filed on is/are: a) ☐ acc		Examiner.			
٠٠/	Applicant may not request that any objection to the					
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority ι	ınder 35 U.S.C. § 119					
a)	Acknowledgment is made of a claim for foreign All b) Some * c) None of:  1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the prio application from the International Burea see the attached detailed Office action for a list	ts have been received. ts have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	on No ed in this National Stage			
2) Notice (3) Inform	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Di 5) Notice of Informal F 6) Other:	ate			

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### **DETAILED ACTION**

1. This office action is in response to the reply filed on 06/30/2009.

2. Claims 7, 10-11, 14, 17, 20-27 and 34-38 are pending in the application and have been examined.

## Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 7, 10-11, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over So (U.S. Patent No. 5,909,559) in view of Assouad (U.S. Patent No. 5,826,093).
- 5. Regarding claims 7 and 14, So discloses an integrated personal computing system comprising:

a central processing unit (CPU106 Fig. l) operable to execute operational instructions, wherein the central processing unit includes an arithmetic logic unit (CPU MMX) interoperably coupled with a data module, an instruction module, wherein the central processing unit issues a memory access request when information relating to executing one of the operational instructions is not stored within the data module or the instruction module (see the IO request and data buffer in col.39, lines 13-60, see also DRAM controller and the arbiter in col.3, lines 11-30, see PCI request from CPU in col.19, lines 9-30), and wherein the central processing unit is contained on a substrate [Fig. 1];

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north bridge [North bridge 108] operably coupled to interface with memory [cache or Main memory] at a memory rate, wherein the north bridge includes a memory access request buffer interoperably coupled with a memory controller [see the RAM and the PCl bus master in col.37, lines 39-67, col.38, lines 1-50], wherein the memory access request buffer receives the memory access request from the central processing unit at the operating rate of the central processing unit, wherein the memory controller retrieves the memory access request from the memory access request buffer [see the IO request and data buffer in col.39, lines 13-60, see also DRAM controller and the arbiter in col.3, lines 11-30, see PCl request from CPU in col.19, lines 9-30] at the memory rate (memory rate not explicitly shown, but must be memory rate otherwise would not be operative), wherein the memory controller processes the memory access request to produce a memory response that includes information stored in memory [see request queue and PCl transactions in col.37, lines 39-67, col.38, lines 1-81, and, a bus operably coupled to the central processing unit [CPU 106] and the north bridge [see connection between CPU 106 and north bridge 108 in fig.l], wherein the bus provides a transport medium for memory access requests and corresponding memory responses between the central processing unit and the north bridge using a native protocol to the central processing unit [in order for the bus to communicate with the processing unit, it must use a protocol that the processing unit also uses or they would not be able to communicate], and wherein the bus is contained on the substrate [Fig. 1].

So does not explicitly disclose that the Northbridge is integrated into the substrate.

Assouad discloses a memory controller within the integrate circuit (col 2 lines 43-49). So would have been motivated to allow an integrated memory controller for performance and efficiency advantages. It would have been obvious at the time of the invention for one of ordinary skill in

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the art to take the processing system of So and incorporate the Northbridge on an integrated circuit, as in Assouad.

6. Regarding claims 10 and 17, So does not explicitly disclose the physical address as claimed. However, since no specific format of physical address has been reflected in the claim, examiner holds that generation of physical address in general had been known in the art.

7. Regarding claim 11, So also included a memory bus coupled to north bridge [see bus connected to the north bridge and the memory in fig. 1].

# Allowable Subject Matter

8. Claims 20-27 and 34-38 are allowed.

## Response to Arguments

9. Applicant's arguments filed 06/30/2009 have been fully considered but they are not persuasive. In attempting to overcome the prior art, applicant has amended the claims to recite that the bus between the central processing unit and the north bridge uses "native protocol to the central processing unit". The examiner respectfully submits that such operation is inherent in the prior art because, if the bus used a protocol that was not native to the CPU, then the CPU would not be able to communicate with the bus and the system would not function as disclosed. It is therefore a functional necessity that the bus used to communicate with the CPU uses a protocol native to the CPU. Applicant's argument is therefore not persuasive.

#### Conclusion

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10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/ Supervisory Patent Examiner, Art Unit 2183 /Corey S Faherty/ Examiner, Art Unit 2183 Page 6